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**PATENT APPLICATION**

**Inventors:** Philip W. Diodato  
Chun-Ting Liu  
Ruichen Liu

**Case** 8-35-22

**Serial No.** 09/742,314

**Group Art Unit** 2815

**Filed** December 21, 2000

**Examiner** J.H. Nguyen

**Title** Inter-Wiring-Layer Capacitors

7/A  
5-7-02  
T. Flowers

**ASSISTANT COMMISSIONER FOR PATENTS  
WASHINGTON, D.C. 20231**

**SIR:**

**Amendments**

This reply is in response to the Official Action mailed December 27, 2001.

**IN THE CLAIMS**

Please cancel claims 9-24 without prejudice.

**Remarks**

Claims 1-8 are currently pending in this application. Claims 9-24 are canceled without prejudice in response to the Examiner's restriction requirement.

The Examiner rejected applicants' claims 1, 2 and 7, stating that the claims are anticipated under 35 USC § 102(e). The Examiner cited US Patent No. 6,180,976 to Roy (Roy hereinafter) as the basis for the rejection.

Applicants' invention is an integrated circuit that consists of a semiconductor substrate with semiconductor devices formed therein and thereon, a first wiring layer located over the substrate, a second wiring layer located on the first wiring layer, and a capacitor. The capacitor has metal-based charge-storage electrodes that extend through